Abstracts

A 50 GHz monolithic RSFQ digital phase locked loop

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HYPRES has developed a monolithic on-chip phase-locked loop (PLL) for the stabilizing and locking of the high-frequency output of an single flux quantum (SFQ) clock source, using rapid single flux quantum (RSFQ) logic family elements for phase detection and frequency detection. This PLL was successfully fabricated and operated as a 50 GHz clock phase-locked to a MHz frequency external source. We were able to employ a feedback loop filter to correct the voltage bias on the SFQ clock and compensate for the frequency fluctuations created by voltage noise in the bias and shunt resistors. This effort resulted is a stable SFQ clock which is tunable and phase-locked to an external signal of lower frequency, and which does not increase the heat load of a circuit. Moreover, in addition to high speed synchronized clock sources, this PLL can now be used to implement new and useful devices, such as phase demodulators and clock recovery circuits.

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